ABSTRACT

The present invention is a flash memory manufacturing process that facilitates efficient fabrication of a flash memory cell. In one embodiment, a silicide (e.g., CoSi) is utilized as a diffusion source. A layer of silicide is deposited over a source area and drain area. The dopant is implanted into the CoSi and diffuse out conformably along CoSi-Si interface at a relatively low temperature. The low temperature diffusion facilitates fabrication of a Flash core cell with a very shallow source/drain junction, and as a result a robust DIBL. The present invention also facilitates fabrication of memory cells with smaller spacers and shorter gate length.